

**ABSTRACT**

A memory device and the method for manufacturing same is disclosed. The device comprises a first oxide layer on top of a substrate, a floating gate layer on top of the first oxide layer, a second oxide layer over the floating gate layer, wherein the second oxide layer and the floating gate layer have a first opening and a second opening respectively, and wherein the width of second opening is bigger than the width of the narrowest region of the first opening so that the floating gate layer is pulled back horizontally underneath the second oxide layer. A source region is in the substrate underneath the first oxide layer, and a third oxide layer fills in the first and second openings conforming to the contour thereof, wherein the third oxide has a third opening to reach a portion of the source region. Further, a control gate material fills in the third opening.